IN THE CLAIMS

Please amend the claims as follows:

Claims 1-15 (Canceled).

Claim 16 (Currently Amended): A process for forming an integrated circuit structure comprising:

forming a layer of dielectric material on a substrate;

forming a layer of tunable etch resistant anti-reflective (TERA) material on said layer of dielectric material; and

~~forming a layer of light-sensitive material on said layer of TERA material, wherein the optical properties of said light-sensitive layer and said layer of TERA material are substantially the same; and~~

forming a dual damascene structure for a metal interconnect, said dual damascene structure having a bottom opening extending to a surface of the substrate, and a top opening in communication with and wider than the bottom opening and extending to said layer of TERA material, wherein, ~~by using~~ said layer of TERA material is etched to a width of the top opening and used as at least one of a lithographic structure for the formation of the interconnect structure, a hard mask, an anti-reflective coating, and a chemical mechanical polishing (CMP) stop layer.

Claim 17 (Currently Amended): The process of Claim 16, further comprising:

forming a layer of light-sensitive material on said layer of TERA material, wherein the optical properties of said light-sensitive layer and said TERA layer are substantially the same;

and

exposing said layer of light-sensitive material to a pattern of radiation,

wherein said forming said layer of TERA material facilitates producing a pattern in said layer of light-sensitive material substantially the same as said pattern of radiation.

Claim 18 (Original): The process of claim 17, wherein said forming said layer of TERA material comprises providing a part of the lithographic structure for the formation of a metal interconnect for said device structure.

Claim 19 (Original): The process of claim 17, wherein said forming said layer of TERA material comprises depositing said layer of TERA material using at least one of chemical vapor deposition (CVD), and plasma enhanced CVD.

Claims 20-21 (Canceled).

Claim 22 (Original): The process of Claim 21, wherein said forming a damascene structure comprises integrating a tunable anti-reflective coating with a dual damascene structure formed using a method comprising at least one a via-first method, a full-via-first method, a full-via with no stop layer method, a trench-first method, and a buried via mask method.

Claim 23 (Withdrawn): A method of forming an interconnect structure comprising:

preparing a film stack comprising a substrate having a metal line, a metal cap layer formed on said substrate, a first dielectric layer formed on said metal cap layer, a second dielectric layer formed on said first dielectric layer, a hard mask layer formed on said

dielectric layer, a tunable etch resistant anti-reflective (TERA) coating formed on said hard mask layer, and a first layer of light-sensitive material formed on said TERA coating;

forming a first pattern in said first layer of light-sensitive material;

transferring said first pattern to said TERA coating;

forming a second layer of light-sensitive material on said TERA coating;

forming a second pattern in said second layer of light-sensitive material;

transferring said second pattern to said TERA coating;

transferring said first pattern to said hard mask layer;

transferring said first pattern to said second dielectric layer;

transferring said second pattern to said hard mask layer;

transferring said second pattern to said second dielectric layer;

transferring said first pattern to said first dielectric layer; and

transferring said first pattern to said metal cap layer.

Claim 24 (Withdrawn): The method of claim 23, further comprising:

removing said first layer of light-sensitive material.

Claim 25 (Withdrawn): The method of claim 23, further comprising:

removing said second layer of light-sensitive material.

Claim 26 (Withdrawn): The method of claim 23, further comprising:

preparing said film stack with an etch stop layer formed on said first dielectric layer prior to said second dielectric layer formed on said etch stop layer; and

transferring said first pattern to said etch stop layer.

Claim 27 (Withdrawn): The method of claim 23, further comprising:

forming a layer of bottom anti-reflective coating (BARC) on said TERA coating; and

removing said BARC layer.

Claim 28 (Withdrawn): A semiconductor device comprising:

a semiconductor substrate;

a film stack formed on the semiconductor substrate; and

means for integrating a tunable anti-reflective coating with a damascene structure for a metal interconnect formed in the film stack.

Claim 29 (Withdrawn): A method of forming an interconnect structure comprising:

preparing a film stack comprising a substrate having a metal line, a metal cap layer formed on said substrate, a first dielectric layer formed on said metal cap layer, a second dielectric layer formed on said first dielectric layer, a hard mask layer formed on said dielectric layer, a first tunable etch resistant anti-reflective (TERA) coating formed on said hard mask layer, a second TERA coating formed on said first TERA coating, and a first layer of light-sensitive material formed on said TERA coating;

forming a first pattern in said first layer of light-sensitive material;

transferring said first pattern to said second TERA coating;

forming a second layer of light-sensitive material on said TERA coating;

forming a second pattern in said second layer of light-sensitive material;

transferring said second pattern to said first TERA coating;

transferring said second pattern to said hard mask layer;

transferring said second pattern to said second dielectric layer;

transferring said second pattern to said first dielectric layer;

transferring said first pattern to said first TERA coating;

transferring said first pattern to said hard mask layer;

transferring said first pattern to said second dielectric layer; and

transferring said second pattern to said metal cap layer.

Claim 30 (Withdrawn): The method of claim 29, further comprising:

removing said first layer of light-sensitive material following said transferring said first pattern to said second TERA coating.

Claim 31 (Withdrawn): The method of claims 29, or 30, further comprising:

removing said second layer of light-sensitive material following said transferring said second pattern to said second dielectric layer.

Claim 32 (Withdrawn): The method of claims 29, 30, or 31, further comprising:

preparing said film stack with an etch stop layer formed on said first dielectric layer prior to said second dielectric layer formed on said etch stop layer; and

transferring said second pattern to said etch stop layer.

Claim 33 (Withdrawn): A method of forming an interconnect structure comprising:

preparing a film stack comprising a substrate having a metal line, a metal cap layer formed on said substrate, a first dielectric layer formed on said metal cap layer, a tunable etch resistant anti-reflective (TERA) coating formed on said first dielectric layer, and a first layer of light-sensitive material formed on said TERA coating;

forming a first pattern in said first layer of light-sensitive material;

transferring said first pattern to said TERA coating;

forming a second dielectric layer on said TERA coating;

forming a second TERA coating on said film stack;

forming a second layer of light-sensitive material on said second TERA coating;

forming a second pattern in said second layer of light-sensitive material;

transferring said second pattern to said second TERA coating;

transferring said second pattern to said second dielectric layer;

transferring said first pattern to said first dielectric layer; and

transferring said first pattern to said metal cap layer.

Claim 34 (Withdrawn): The method of claim 33, further comprising:

forming a hard mask layer on said second dielectric layer; and

forming said second TERA coating on said hard mask layer; and

transferring said second pattern to said hard mask layer.

Claim 35 (Withdrawn): A method of forming an interconnect structure comprising:

preparing a film stack comprising a substrate having a metal line, a metal cap layer formed on said substrate, a first dielectric layer formed on said metal cap layer, a hard mask formed on said first dielectric layer, a tunable etch resistant anti-reflective (TERA) coating formed on said hard mask layer, and a first layer of light-sensitive material formed on said TERA coating;

forming a first pattern in said first layer of light-sensitive material;

transferring said first pattern to said TERA coating;

transferring said first pattern to said hard mask layer;

transferring said first pattern to said first dielectric layer;

transferring said first pattern to said metal cap layer;

removing said TERA coating;

filling said first pattern in said first dielectric layer and said metal cap layer with metal;

forming a second metal cap layer on said film stack;

forming a second dielectric layer on said second metal cap layer;

forming a second hard mask layer on said second dielectric layer;

forming a second TERA coating on said second hard mask layer;

forming a second layer of light-sensitive material on said second TERA coating;

forming a second pattern in said second layer of light-sensitive material;

transferring said second pattern to said second TERA coating;

transferring said second pattern to said second hard mask layer;

transferring said second pattern to said second dielectric layer; and

transferring said second pattern to said second metal cap layer.

Claim 36 (Currently Amended): The process of claim 16, wherein said forming a dual damascene structure comprises using said layer of TERA material as a hard mask for forming the top opening of the dual damascene structure.

Claim 37 (Currently Amended): The process of claim 16, wherein said forming a dual damascene structure comprises using said layer of TERA material as a sacrificial layer for forming said top opening of the dual damascene structure.

Claim 38 (Currently Amended): The process of Claim 16, wherein said forming a dual damascene structure comprises using said layer of TERA material as a CMP stop layer for forming said top opening of the dual damascene structure.

Claim 39 (New): The process of Claim 16, wherein said forming a dual damascene structure comprises first etching the layer of TERA material to the width of the bottom layer, and then etching the layer of TERA material to the width of the top layer.

Claim 40 (New): The process of Claim 16,

forming another layer of TERA material in the layer of dielectric material; and

etching the another layer to a width of the bottom opening.